K/*Ka*-Band Low-Noise Embedded Transmission Line (ETL) MMIC Amplifiers

Hua-Quen Tserng, *Fellow, IEEE*, Larry C. Witkowski, *Member, IEEE*, Andrew A. Ketterson, *Member, IEEE*, Paul Saunier, *Senior Member, IEEE*, and Ted Jones, *Member IEEE*

***Abstract*— The design, fabrication, and performance of producible, high-performance K- and Ka-band pHEMT low-noise MMIC amplifiers using the embedded transmission line (ETL) circuit concept with top-side grounding are reported. A state-of-the-art noise figure of 1.2 dB with 25-dB gain is achieved at 31 GHz. These amplifiers can be implemented in low-cost, ultra-compact receiver modules for emerging spaceborne phased-array communication applications.**

***Index Terms*— MMIC amplifiers, MMIC receivers, MMIC's, MODFET amplifiers.**

I. Introduction

THE embedded transmission line (ETL) MMIC approach first reported in [1] utilizes matching circuits with transmission lines and lumped passive components (resistors, series/shunt capacitors, and spiral inductors) embedded in a low-K dielectric (polyimide) medium coated over the active devices. Our new ETL MMIC approach has the potential of revolutionizing multichip assembly in terms of packing density, performance, and cost. Among the advantages are: chip-scale packaging with no bond wires (quasi-hermetic, small size, no external package), ease of encapsulation, and suitability for high-density interconnects with minimum mounting parasitic. Potential application areas include: phased array antennas for mobile satellite communication, phased array radar, low-cost, high-density multichip modules for wireless communications, and millimeter-wave radios. In this paper, highly uniform performance from a K-band low-noise amplifier (LNA) design and state-of-the-art noise performance from a Ka-band MMIC design are reported. These low-noise amplifiers are critical receiver components for emerging satellite communication applications at K-and Ka-band frequencies.

II. Embedded Transmission Line (ETL) MMIC Technology

The ETL MMIC approach uses matching circuits with transmission lines and lumped passive components embedded in a low-K dielectric (such as polyimide) medium. Fig. 1 shows the sketch of an ETL MMIC cross section with an unthinned GaAs substrate. The MMIC can be used either upright (top-side ground with the GaAs substrate down) or in inverted configuration with flipped transistors for efficient heat transfer and low common-lead inductance. This approach differs from the traditional MMIC design in that transistor sources (FET) or emitters [bipolar junction transistors (BJT's)] are individually grounded to the top-side ground plane (through plated heatsink over source or emitter interconnect bridges) to provide excellent heat transfer (in inverted configuration) and low-inductance ground connections. Other passive components such as transmission lines, resistors, and capacitors are fabricated on the GaAs as before; they are redesigned taking into account the new circuit configuration with mixed dielectric (i.e., low-K dielectric and GaAs substrate). Shunt components such as MIM capacitors and/or shorted transmission line stubs are readily grounded through gold plugs in the thin dielectric rather than the GaAs substrate as in the conventional MMIC approach. The thickness of the dielectric layer can be on

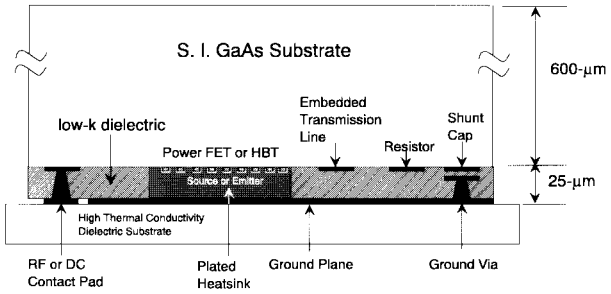

Fig. 1. ETL power MMIC with flipped transistor.

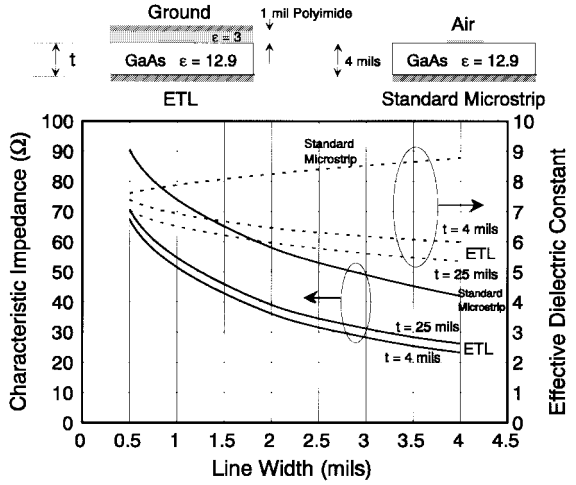

Fig. 2. Transmission-line characteristics.

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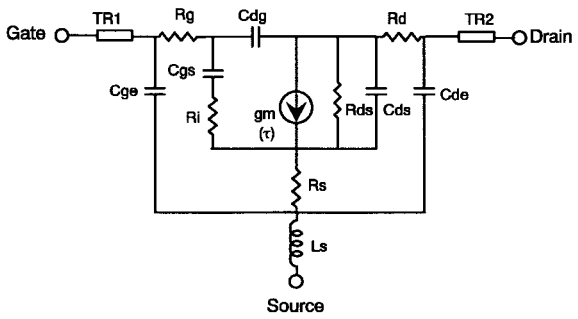

Rg	Ri	Cgs	Cdg	gm	Tau	Rs	Rds	Cds	Rd	Ls	Cge	Cde
5.73	0.76	0.21	0.026	75.7	1.37	2.48	473	0.037	0.97	0.004	0.11	0.009

Fig. 3. Equivalent circuit model of a 150-μm gatewidth pHEMT at low-noise bias.

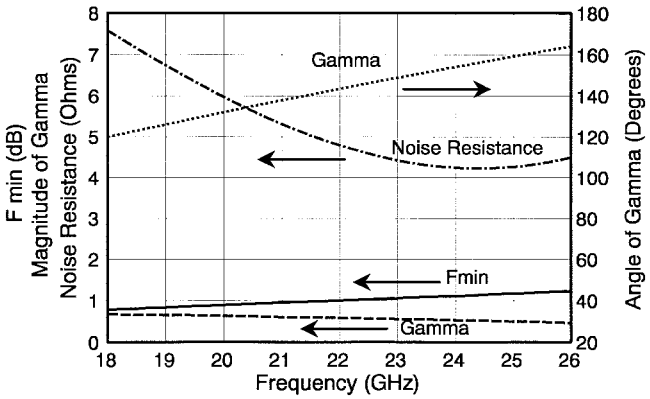

Fig. 4. Noise parameters of a 150-μm pHEMT ($V_d = 3$ V, $V_g = +0.3$ V, $I_d = 10$ mA).

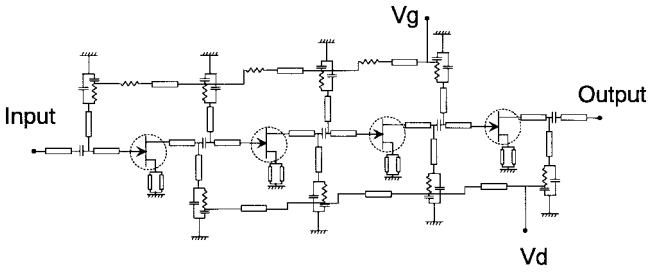

Fig. 5. Four-stage K-band low-noise amplifier circuit.

the same order as the plated source/emitter (25–50 μm). For RF I/O and dc biases, connecting pads are isolated from the top-side ground plane, allowing for on-wafer testing and versatile interconnections to other module components through multilayer interconnect board. In the configuration shown in Fig. 1 with unthinned substrate, no through-GaAs substrate vias (as in the conventional MMIC case) are required for the shunt components, which greatly simplifies the process and reduces the costs. If desired, the substrate can be thinned to provide an extra ground plane and through-wafer vias. This allows desirable I/O pads for vertical integration with other ETL MMIC chips or multilayer interconnect/distribution boards. The I/O and bias pads can be provided either through GaAs substrate or the polyimide layer. For thickness compatibility with other module components, the ETL MMIC chips described in this paper use 4-mil (100-μm) thick GaAs with 1-mil (25-μm) thick polyimide and double-sided ground plane.

The characteristics of ETL's were obtained using 3-D electromagnetic simulator software. Fig. 2 shows the characteristic impedance and effective dielectric constant of conventional microstrip transmission lines (with 4-mil-thick GaAs substrate) and ETL's with a 1-mil-thick polyimide layer (dielectric constant $= 3$) for two GaAs substrate thicknesses (4 and 25 mils). As expected, the effect of the thin polyimide layer with its associated ground plane is to lower the characteristic impedance and effective dielectric constant for a given conductor width. For the ETL with 4-mil thick GaAs, the line width for a 50-Ω characteristic impedance is about 1 mil (25 μm). As shown, there is a very weak dependence of the impedance and effective dielectric constant on the thickness of the GaAs substrate.

III. Low-Noise ETL MMIC Design and Performance

AlGaAs/InGaAs on GaAs pseudomorphic high electron mobility transistor (pHEMT) with channel structure optimized for low-noise performance at K/Ka-band was used. The design features 0.25-μm long T-gate with etch-stop layer for recess uniformity and high yield. The MMIC design is based on 25-μm thick polyimide and 4-mil (100-μm) thick GaAs substrate. RF on-wafer S-parameters, and noise parameters were measured for both discrete devices and MMIC amplifiers. Fig. 3 shows the equivalent circuit model of a 150-μm gatewidth ETL pHEMT biased for low-noise operation. The units are: resistor (Ω), capacitor (pF), inductor (nH), transconductance (mS), time (pS). The minimum noise figure is obtained at a gate bias of $+0.3$ V with a drain voltage of 3 V and drain current of 10 mA. The intrinsic transconductance is as high as 505 mS/mm. Fig. 4 shows the measured noise parameters ($F_{\min}$, R_n, and Γ_{opt}) of the 150-μm gatewidth device over 18 to 26 GHz band. The minimum noise figure is about 1 dB at 21 GHz. The associated gain (not shown) is about 9 dB at the same frequency. A simplified schematic circuit diagram of the four-stage K-band amplifier is shown in Fig. 5. This circuit features high-impedance transmission lines,

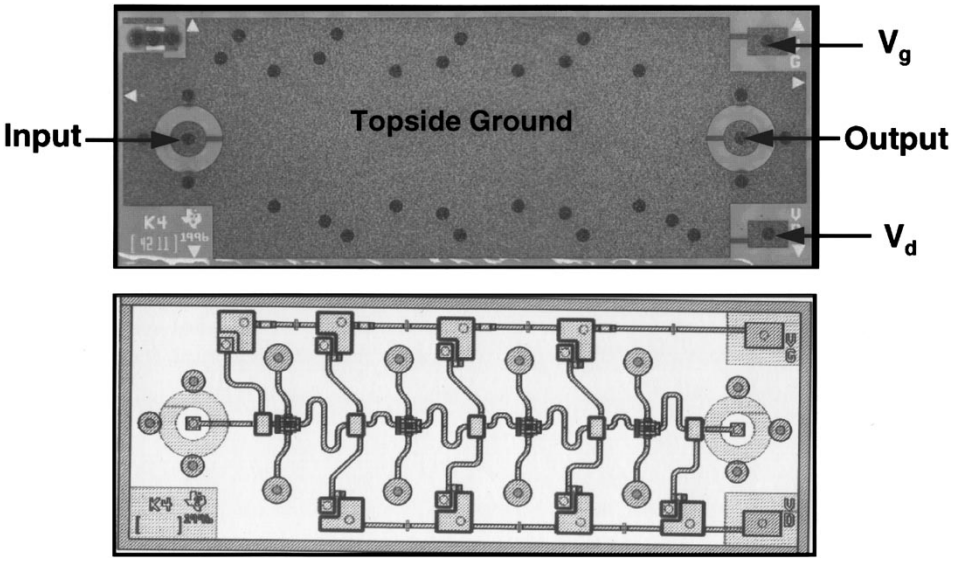

Fig. 6. A four-stage K-band ETL MMIC low-noise amplifier.

MIM dc-blocking and RF bypass capacitors, and necessary bias stabilization RC networks for both in-band and out-of-band stabilization. A series feedback source inductance is used in each stage for stability. It also provides simultaneous noise and conjugate match for the input of the first stage. For the ETL circuit design, the characteristic impedance and effective dielectric constant of embedded transmission lines of various widths were obtained using a 3-D electromagnetic simulator software. Fig. 6 shows the K-band four-stage ETL MMIC low-noise amplifier with 150 μm gate width pHEMT in each stage. It measures 60 mils $\times$ 162 mils (no attempts were made to minimize the chip size for the first pass design). The top picture shows the top-side ground with RF I/O's and bias pads. The bottom picture shows the underlying circuitry with the top 25-μm thick polyimide layer removed. With the exception of RF input/output pads and gate/drain pads, a solid ground plane is provided for ease of connecting to other components (i.e., solder bumps) without using bondwires. This approach results in minimum mounting parasitic and lower assembly cost. Unlike most other reported bias approaches with separately biased first and subsequent stages for achieving low noise and high gain, we use a single gate voltage and a single drain voltage for all stages (through on-chip bias networks) to simplify power supply requirement for module integration. As discussed earlier, on-wafer noise characterization was used for both discrete devices and MMIC amplifiers. Only a slight modification of conventional MMIC fabrication technique is required for ETL MMIC fabrication [2]. The process steps are identical up to the source interconnect level. Then, a thin layer of polyimide is applied and the first plated-metal interconnect layer is formed. Plated 25-μm height gold via "plugs" are then formed to connect the device sources and capacitors (shunt) to the ground plane. The required I/O's and bias vias are also formed at this point. A thick polyimide dielectric is then spin coated and cured to a thickness of 25 μm. Planarization and dielectric thickness control is achieved through mechanical lapping of the polyimide. Fig. 7 shows a photograph of array of ETL MMIC amplifiers on a wafer. As mentioned earlier,

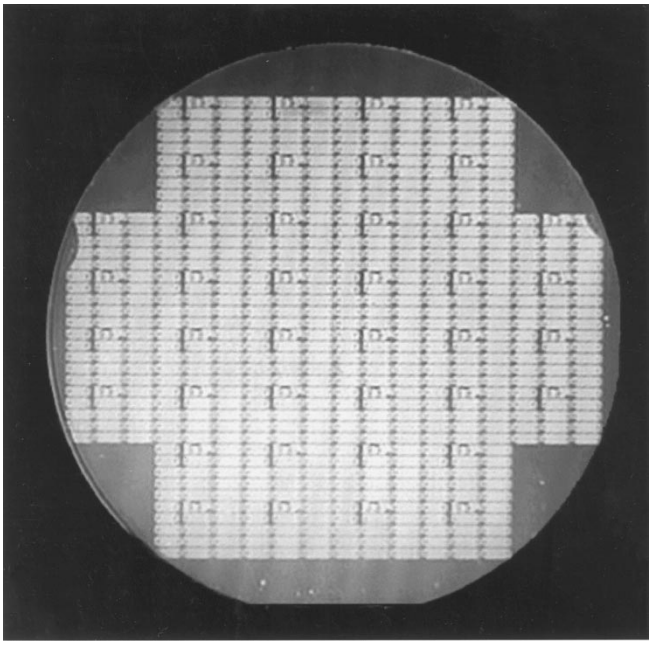

Fig. 7. ETL LNA's in wafer form.

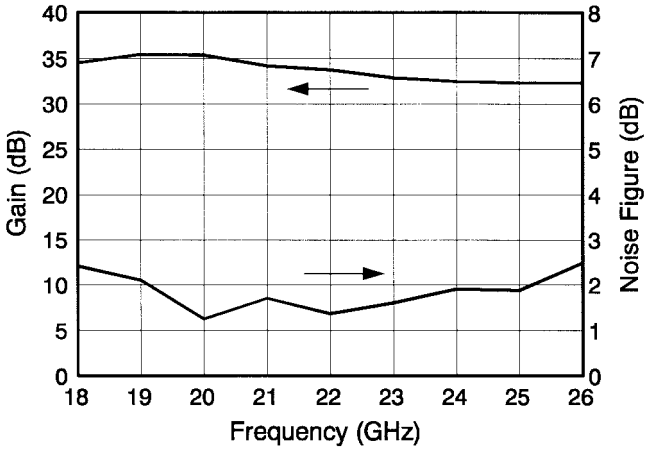

Fig. 8. Performance of four-stage ETL MMIC LNA.

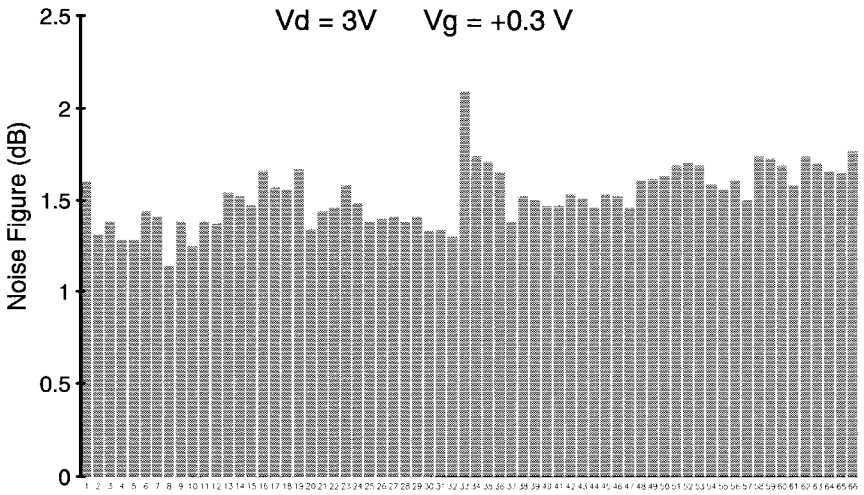

Fig. 9. Noise figure distribution of 66 ETL K-band LNA chips at 20 GHz.

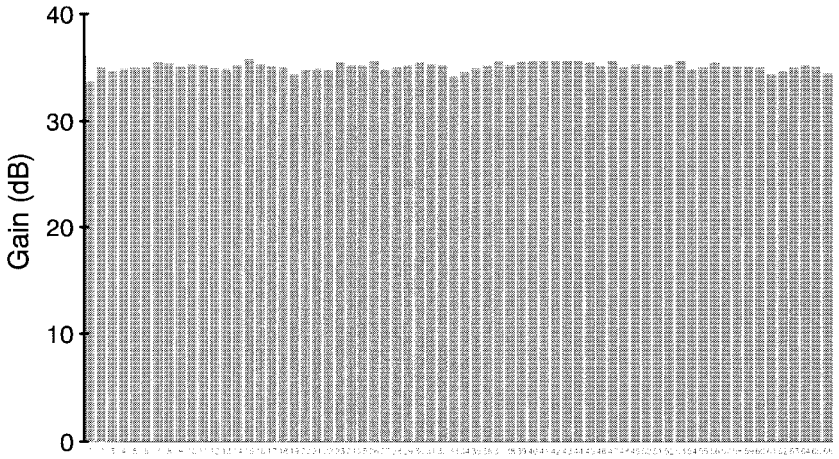

Fig. 10. Gain distribution of 66 K-band LNA chips.

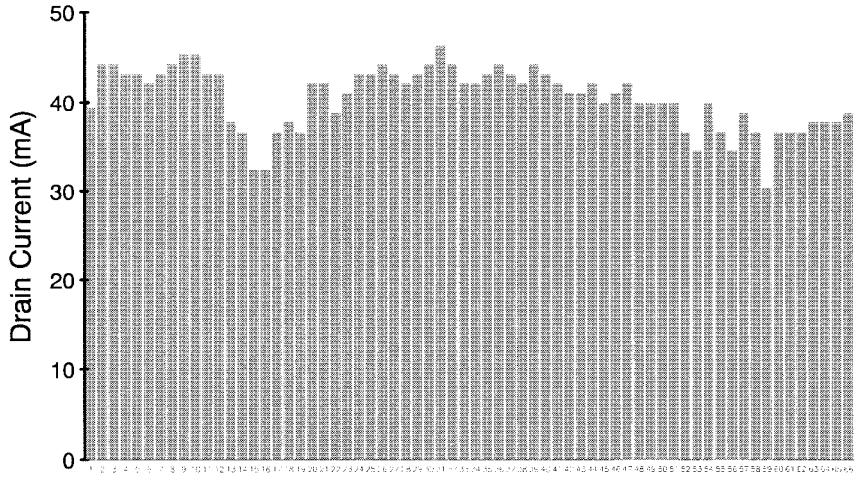

Fig. 11. Drain current distribution of 66 K-band LNA chips.

except for the RF I/O's and bias pads, the photograph shows the top-side ground plane readily integratable with other module components.

Fig. 8 shows the gain/noise figure performance of a typical chip. Over most of the 18–26 GHz frequency band, the noise figure remains below 2 dB with the lowest noise figure of 1.3 dB at 20 and 22 GHz (the amplifier design was optimized for 20–22 GHz operation). The gain remains above 33 dB over the same band. Figs. 9–11 show, respectively, the 20 GHz noise figures, gains, and drain currents of 66 four-stage amplifier

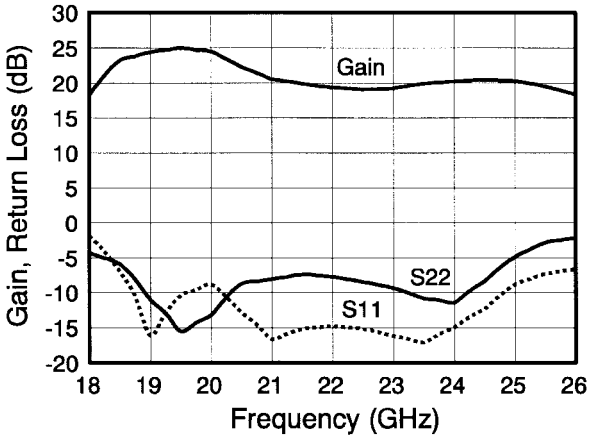

Fig. 12. Performance of a three-stage ETL MMIC amplifier with thick GaAs substrate.

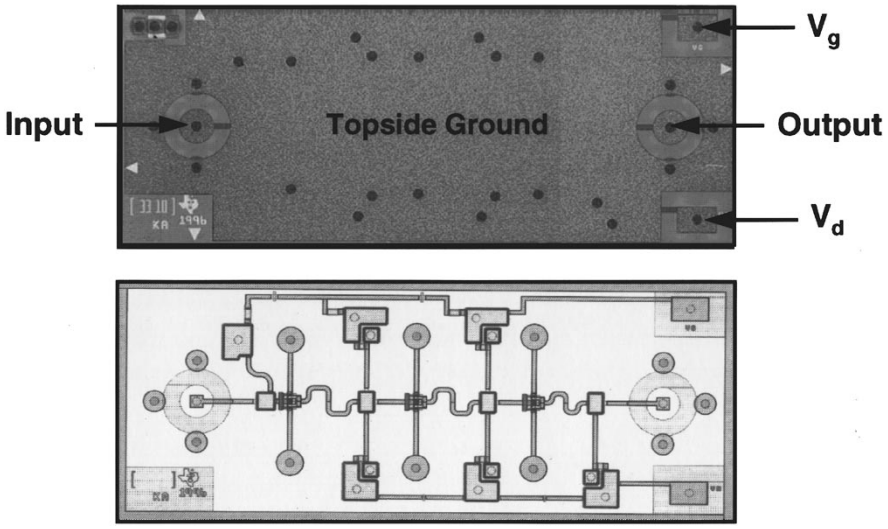

Fig. 13. Three-stage Ka-band ETL MMIC low-noise amplifier (60 × 148 mils).

chips from the same wafer. The use of etch-stop layer for the channel recess has resulted in a remarkable uniformity across the wafer. The average noise figure is about 1.5 dB with the best noise figure of 1.2 dB. The average gain is 35 dB. It should be noted that all amplifiers were biased at a drain voltage of 3 V and a gate voltage of +0.3 V. A three-stage version of the K-band LNA MMIC achieved a gain of 25 dB with similar noise figure as that of a four-stage amplifier.

The ETL MMIC amplifiers with the results described above have double-sided ground plane with thin (4-mil) GaAs substrate. Other ETL MMIC's being developed in our laboratory use thick (∼25 mils) GaAs substrate for lower production cost. The gain performance of one three-stage K-band ETL MMIC wafer with unthinned GaAs (∼25-mil thick) was measured. Because of a lower than expected transconductance, the noise figure was not measured. Fig. 12 shows the performance across the 18–26 GHz frequency band. Even though the MMIC was designed for thin GaAs, the performance (gain) is still quite good. As can be seen from the ETL impedance plot of Fig. 2, the impedance and effective dielectric constant are not very sensitive to the GaAs substrate thickness between 4- and 25-mil. Fig. 12 shows that the ETL MMIC with thick GaAs substrate is a viable approach for lower processing cost, since no backside processing of GaAs is required.

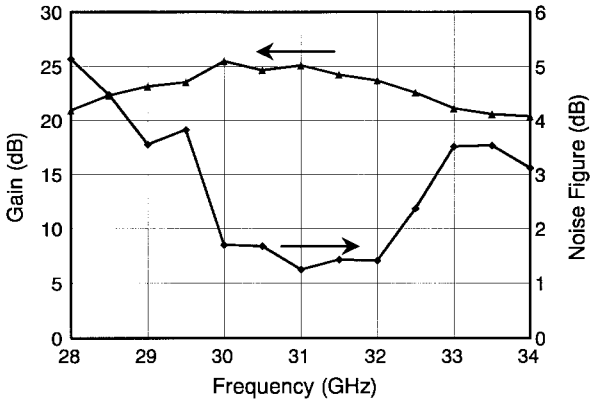

Fig. 14. Performance of a three-stage Ka-band ETL MMIC low-noise amplifier ($V_d = 3$ V, $V_g = +0.41$ V, $I_d = 35.6$ mA).

Fig. 13 shows a three-stage Ka-band ETL MMIC low-noise amplifier. The top picture shows the upper ground plane with RF I/O's and dc bias pads. The bottom picture shows the underlying circuitry with the top polyimide layer ($\sim$25 μm thick) removed. For this MMIC, the GaAs substrate is 4-mil thick. The chip measures 60 $\times$ 148 mil. Like the K-band design, no attempts were made in this first pass design to minimize the chip size. Obviously, up to 30%–40% reduction in chip size is possible to increase the number of chips per wafer. Low-noise 0.25-μm long T-gate pHEMT with 100-μm gatewidth is used in each stage. The circuit topology is similar to that of the K-band amplifier shown in Fig. 5. Fig. 14 shows the gain and noise figure performance. A state-of-the-art noise figure of 1.2 dB with 25-dB gain is achieved at 31 GHz. The noise figure is less than 2 dB between 30 and 32 GHz. Similar to that of the four-stage K-band amplifier (Fig. 6), on-chip gate and drain bias networks are used for single drain and single gate power supply operation. Our ETL MMIC noise figure results compare favorably (1 dB noise figure at 32 GHz) with the reported conventional Ka-band MMIC amplifier results using 0.15-μm gate length pHEMT's [3]. Our noise figure is lower than that reported in [4] for a Ka-band MMIC LNA using 0.2-μm gate length pHEMT's.

IV. Conclusions

The K/Ka-band low-noise ETL MMIC amplifiers reported in this paper can be used in low-cost, ultra-compact receiver modules for emerging spaceborne phased-array communication applications. The chip-scale packaging nature of the ETL MMIC having I/O's and bias pads suitable for flip-chip mounting (using either solder bumps or Z-axis adhesives) can simplify or even eliminate bulky and expensive packages for low-cost phased array antenna applications.

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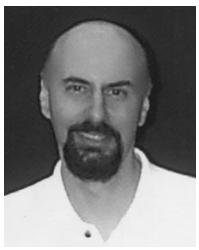

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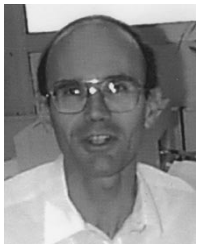

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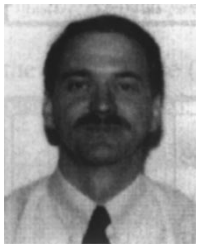

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